McGINN & GIBB, PLLC
A PROFESSIONAL LIMITED LIABILITY COMPANY
PATENTS, TRADEMARKS, COPYRIGHTS, AND INTELLECTUAL PROPERTY LAW
8321 OLD COURTHOUSE RD, SUITE 200
VIENNA, VIRGINIA 22182-3817
TELEPHONE (703) 761-4100
FACSIMILE (703) 761-2375

APPLICATION
FOR
UNITED STATES
LETTERS PATENT

APPLICANT: Bojarczuk, Jr. et al.

FOR: METHOD OF FORMING LATTICE-
MATCHED STRUCTURE ON SILICON
AND STRUCTURE FORMED
THEREBY

DOCKET NO.:   YOR920010368US2

METHOD OF FORMING LATTICE-MATCHED STRUCTURE ON SILICON AND STRUCTURE FORMED THEREBY

CROSS-REFERENCE TO RELATED APPLICATIONS

5

The present application is a continuation-in-part of U.S. Patent Application Serial No. 09/898,039, to Bojarczuk et al., having IBM Docket No. YOR920010368US1, filed on July 5, 2001, incorporated herein by reference.

BACKGROUND OF THE INVENTION

10

Field of the Invention

The present invention generally relates to an insulator, and more particularly to a lattice-matched epitaxial insulator structure formed on silicon, and arbitrarily grown, lattice-matched epitaxial insulator-silicon and germanium

15 structures grown on top of each other.

Description of the Related Art

Prior to the present invention, there has not been any demonstrated lattice-matched epitaxial insulator structure formed on silicon where the lattice constant of the oxide can be varied arbitrarily so that it is equal to, or an integral multiple of the lattice constant of silicon. However, such

5   lattice-matched epitaxial insulator structures on Si are needed for various reasons.

Firstly, such insulators can be used as gate dielectrics for Si complementary metal oxide semiconductor (CMOS) transistors with the view that an epitaxial structure will be less defective. Such epitaxial structures

10   based on $SrTiO_3$-type perovskite structures have been grown as described in "Crystalline Oxides on Silicon: The First Five Monolayers", Rodney A. McKee et al., Physical Review Letters, Volume 81, Number 14, October 5, 1998, pp. 3014-3017.

However, these structures have a lattice mismatch that is about 2% off

15   from that of Si. These oxide films are grown on Si surfaces that are oriented in the <100> crystalline direction and while they are aligned in the plane of growth to the spacing of the silicon atoms in the <110> directions in the growth plane to a small level of lattice mismatch, they exhibit a large lattice mismatch to the silicon in the direction perpendicular to the growth plane.

20   Epitaxial structures can also be made with Y_2O_3 but the lattice mismatch is about 2.5%.

Secondly, such insulators can be used for fully epitaxial Si/insulator/Si epitaxial structures or epitaxial Ge/insulator/Ge epitaxial structures. There have been no prior reports of successful growth of Si/oxide/Si epitaxial

YOR920010368US2

structures with a flat interfacial and surface profile for thin (less than about 50 nm) epitaxial layers. These structures can be used for a variety of different applications such as, for example, silicon-on-insulator (SOI) structures or germanium-on-insulator (GOI) structures for transistors, double-gated FET structures, and novel optical and optoelectronic devices.

Thus, prior to the invention, gate dielectrics/insulators have been provided that are epitaxial, but not lattice-matched. However, these dielectrics/insulators are still problematic as lattice mismatch induced defects are created in the devices (e.g., CMOS FET) incorporating such structures. These defects act as traps and affect the turn-on of the device (transistor), as well as the stability and mobility of the device.

In addition, prior to the present invention, no Si substrate/epitaxial oxide/epitaxial silicon structures have been grown that have smooth and uniform surfaces and interfaces for ultrathin layer thicknesses (<50 nm). There has been one report (e.g., see "Epitaxial CeO_2 on Silicon Substrates and the Potential of $Si/CeO_2/si$ for SOI Structures", A.H. Morshed et al. Mat. Res. Soc. Symp. V474, 339(1197)) of attempting to grow epitaxial Si films on CeO_2 (cerium oxide). However, the Si growth profile was rough and three dimensional and the silicon was not completely epitaxial in nature.

Thus, prior to the present invention, there has not been any lattice-matched epitaxial insulator-silicon structure formed on silicon which is substantially defect-free and uniform, nor has the advantages of such a structure been recognized prior to the present invention. This is also the case for lattice matched epitaxial insulator-germanium structures.

SUMMARY OF THE INVENTION

In view of the foregoing and other problems, drawbacks, and disadvantages of the conventional methods and structures, an object of the present invention is to provide a lattice-matched epitaxial insulator structure formed on silicon and a method of forming the same.

In a first aspect of the present invention, a method (and resultant structure) of forming a semiconductor structure, includes processing an oxide to have a crystalline arrangement, and depositing an amorphous semiconductor layer on the oxide by one of evaporation and chemical vapor deposition (CVD).

In the present invention, an optimum method is provided for depositing silicon (or other semiconductor) layers on top of the lattice matched oxide layer.

In such a method, the mixed rare earth oxide layer is cooled down to between room temperature and 100 C following which a thin silicon (or other semiconductor) layer is deposited on top of the epitaxial oxide film surface by evaporation. Since the deposition temperature is low, the as-deposited silicon (or other semiconductor) has an amorphous microstructure. A key aspect to this deposition is that the substrate temperature is low enough that the deposited silicon (or other semiconductor) assumes an amorphous microstructure.

Thereafter, the amorphous silicon (or other semiconductor)/oxide/silicon structure is gradually heated up to a temperature where the silicon (or other semiconductor) starts crystallizing epitaxially. In this case, the seed for epitaxial crystallization is provided by the underlying crystalline oxide template.

5   Above approximately 550C, the amorphous silicon (or other semiconductor) layer transforms to a single crystal epitaxial layer due to solid phase epitaxial growth seeded by the oxide surface below.

In order for the solid phase epitaxy to proceed with a smooth silicon (or

10   other semiconductor) surface, the annealing for solid phase epitaxy can be achieved in the presence of a vapor or flux of a surfactant such as antimony.

It is noted that the solid phase epitaxy of silicon (or another semiconductor material) itself is not new. Also, the growth of a semiconductor in the presence of a surfactant is known. Instead, some novel aspects here include :

15   (i) in this case the solid phase epitaxy of the silicon (or other semiconductor) is seeded by this novel crystalline oxide that has been grown underneath, and (ii) also that the solid phase epitaxy on this oxide surface is carried out in the presence of a vapor of a surfactant. The surfactant alters the surface energy of the silicon (or other semiconductor), such that it does not roughen as a result

20   of the solid phase epitaxy.

Once the solid phase epitaxy has proceeded to completion, at the substrate temperature of above about 550 C (or another temperature if another semiconductor is used), the surfactant vapor can be turned off.

The above process can be substantially identically performed with germanium (or a silicon-germanium mixture) instead of silicon to make germanium/oxide heterostructures.

The present inventors have grown Ge and Si by this process on a specific oxide layer (i.e., LaY-oxide and Y-oxide). However, this will work on any crystalline oxide that shares some surface symmetry with Si or Ge. Thus, the invention advantageously provides a unique solid phase epitaxial process where the Si or Ge is grown in this fashion on any such crystalline oxide.

With the unique and unobvious aspects of the invention, a lattice-matched epitaxial insulator structure is formed on silicon. These structures can be used for a variety of different applications such as, for example, silicon-on-insulator structures for transistors, double-gated FET structures, and novel optical devices.

The inventive compound has a lattice constant which is preferably twice that of silicon, and thus it is a multiple such that everything "fits". The insulator also possessed a high band-gap (>5 eV), a high permittivity (>10) and a low electrical current leakage. As a result, various band gap engineered thin film heterostructures with silicon may be conceived. Some of these devices have been mentioned above, but are re-emphasized below.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other purposes, aspects and advantages will be better understood from the following detailed description of a preferred embodiment of the invention with reference to the drawings, in which:

5   Figure 1 illustrates a flowchart of the method 100 according to the present invention;

Figure 2A illustrates a structure 200A of the invention in its most basic form;

Figure 2B illustrates a structure 200B formed by the method 100 of the

10   present invention;

Figure 3 illustrates another structure 300 of the method of the present invention including a multi-layer stack structure; and

Figure 4 illustrates a flowchart of a preferred method of performing a deposition of silicon (and/or Germanium or another semiconductor material) in

15   step 140 of Figure 1.

DETAILED DESCRIPTION OF PREFERRED

EMBODIMENTS OF THE INVENTION

Referring now to the drawings, and more particularly to Figures 1-4, there are shown preferred embodiments of the method and structures

20   according to the present invention.

PREFERRED EMBODIMENT

Prior to turning to the details of the invention, it is noted that the present invention has provided a new material, $(La,Y)_2O_3$ that can be closely matched to the Si lattice for epitaxial growth.

5　　　That is, Yttrium oxide is a well-known oxide which has a cubic bixbyite (e.g., "bixbyite" refers to a specific cubic, crystallographic structure) structure with a lattice constant of 1.06 nm, which is about 2.4% smaller than two times the lattice constant of silicon. As a result, when one grows thin films of Y_2O_3 on silicon, the deposition has epitaxial characteristics but is not of good quality

10　　　(e.g., defects are created).

Further, lanthanum oxide (La_2O_3) is a well-known oxide which has a larger La to O bond length, since La is a larger atom. However, under normal circumstances La_2O_3 crystallizes with a hexagonal structure and cannot be lattice-matched to silicon.

15　　　There has been reported a cubic bixbyite La_2O_3 phase, and it has a lattice constant of 1.138 nm. However, it is not a stable phase under normal pressure and room temperature.

Thus, these known compounds are problematic. The present invention provides a new compound which overcomes the problems of these and other

20　　　compounds, as discussed below.

That is, in the present invention, a new, metastable $(La_xY_{1-x})_2O_3$ alloy has been created. This alloy, at around $x = 0.3$, will be perfectly lattice-matched to silicon and will crystallize in the cubic structure. That is, in its most basic form, as shown in the structure 200A of Figure 2A, includes the novel

YOR920010368US2

compound 230 grown on a silicon substrate 210, as described in further detail below.

In spite of the tendency for La_2O_3 to crystallize hexagonally, the cubic modification occurs due to crystal structure stabilization from the Y-

5   containing oxide and epitaxial stabilization from the Si substrate. At x = 0.33, the lattice constant of the alloy will be 1.086 nm (i.e., exactly the same as Si). This follows from a linear interpolation between the La_2O_3 lattice constant of 1.138nm, the Y_2O_3 lattice constant of 1.06nm, and using Vegard's law.

The present inventors have demonstrated that by straightforward molecular

10   beam epitaxy (MBE), an epitaxial film of good quality may be grown on silicon by depositing $(La_xY_{1-x})_2O_3$. This shows bright, reconstructed reflection high energy electron diffraction patterns typically observed in good epitaxial growth. X-ray diffraction of such layers also indicate that they are epitaxial, single crystal in nature, and of very high quality. It is noted that the invention

15   does not rely on MBE, but instead can employ other types of growth techniques.

Second Embodiment

Further, to the compound described in the first embodiment, in another aspect of the invention, the present inventors have also discovered that, after

20   growing the epitaxial $(La,Y)_2O_3$ layer on silicon (e.g., described below in further detail and shown in step 140 of Figure 1), an epitaxial Si layer can be further grown directly on top of this epitaxial $(La,Y)_2O_3$ layer. Such epitaxial growth can be performed by MBE. This is again clearly observed from in-situ

reflection high energy electron diffraction patterns. These patterns indicate that a smooth, reconstructed silicon surface may be obtained.

This is the first time a silicon/oxide/silicon structure has been grown epitaxially with such a smooth reconstructed surface. The surface however becomes smooth only after about 50 nm of growth, while for many applications, smooth layers much thinner than this are required. Additionally, these thick layers contain large densities of extended defects.

Example

Turning to Figure 1, the method 100 of the invention will be described hereinbelow.

First, in step 110, a wafer was prepared. That is, a clean Si wafer was taken and dipped in a hydrofluoric acid solution in order to produce a hydrogen-passivated surface. The wafer orientation is preferably <111>, but it can also be <100> or <110>. The wafer may have a thickness within a range of about 1 μm to about 10000 μm. However, it is noted that any thickness may be used, as the thickness of the wafer is not relevant to the invention. Alternatively, one Si wafer may not be hydrogen passivated and can retain a thin (2nm or less) silicon dioxide layer on its surface.

Then, the wafer was loaded into a vacuum deposition system and heated to about 600 C in order to desorb the H from the surface and clean it up. It is also possible to heat the wafer to 1000°C to clean it further, but such a step is not critical.

Following preparation of the Si surface, in step 120, an epitaxial Si buffer was grown on top of the Si wafer resulting in a clean and smooth surface. However, this step is not essential for the process (e.g., the Si buffer layer is optional).

5   If the silicon buffer layer is grown, then the starting surface should be a clean, oxide-free surface. On the other hand, if the L_aY oxide is to be deposited, then it could be deposited directly on top of the thin (<2nm) silicon oxide, or on an oxide-free silicon surface. In this example of the present invention, the vacuum chamber for deposition was a standard molecular beam

10   epitaxy chamber. The buffer layer may have a thickness within a range of about 0.5nm to about 1 micron or more.

In step 130, the $(La,Y)_2O_3$ (or another mixed rare earth oxide as mentioned below) is now ready for deposition. La and Y are heated using standard high temperature commercial effusion cells. Typical La and Y cell

15   operation temperatures are 1300-1700 C. Depending upon the specific cell temperature, the element fluxes can be controlled (as is typical in a standard molecular beam deposition process) and thereby the relative composition of La:Y can be controlled in the deposited film. Oxygen is provided by a molecular oxygen beam. Alternatively, radio frequency (RF) excited atomic

20   oxygen can be provided as well, or in place of molecular oxygen.

With the La and Y cells raised to the appropriate temperature, and an oxygen flow rate of about 1-3 sccm, so that the chamber pressure is in about the 1E-5 to 1E-4 range, the epitaxial growth of $(La,Y)_2O_3$ was commenced by opening the La and Y shutters with the substrate facing all three sources (e.g.,

La, Y, and O). The substrate temperature is typically about 650C, but can be anywhere in the 400-800C range. Epitaxial growth of $(La,Y)_2O_3$ now occurred. Films have been grown with compositions from $0<x<0.5$ for the compound $(La_xY_{1-x})_2O_3$. The lattice matching occurs at around $x = 0.3$.

5   Remarkably, single crystal films will grow even through a thin S_iO_2 layer is on the Si surface

When the Si wafer orientation was (001), the LaY-oxide was grown with its (011) direction normal to the film surface. When the Si wafer orientation was (011), the LaY-oxide was grown with its (111) direction

10   normal. When the Si wafer orientation was (111), the LaY-oxide orientation was normal to the film surface was (111).

Therefore, in the first case, one obtains a two domain epitaxial growth, and in the other two cases, it is possible to get true epitaxial growth.

For epitaxial deposition on Si(111), near-lattice matched LaY-oxides

15   may be grown with a (222) x-ray diffraction full width at half maxima of about 130 arc seconds which indicates the high quality nature of the growth. The inventive compound $(La_xY_{1-x})_2O_3$ may have a thickness within a range of about 0.5nm to more than 1 micron. Again, the thickness thereof is not relevant to the invention.

20   Following deposition of the oxide, the vacuum chamber was pumped down to about 10^{-9} torr to reduce background oxygen pressures.

Then, in step 140, epitaxial silicon was deposited onto the oxide surface by keeping the substrate at 650 - 700 C and evaporating the Si from an electron beam source. The silicon was deposited epitaxially as clearly observed from

YOR920010368US2

reflection high energy electron diffraction images. The epitaxial silicon layer may have a thickness within a range of about 0.5nm to about more than 1μm. Again, the thickness is not relevant.

Hereinabove, a general method is described for depositing silicon (or another semiconductor) layers on top of the lattice matched oxide layer.

That is, while the above description generally describes depositing the silicon (or other semiconductor) epitaxially, hereinbelow and with reference to the flowchart of Figure 4, a specific example of depositing this silicon epitaxially is provided which the present inventors have shown to be optimum thus far. It is noted that for ease of description below, silicon will be assumed to be the semiconductor material used, but of course as mentioned above and below, other materials can be used including germanium, or a mixture of germanium and silicon.

Thus, the invention provides a solid phase epitaxy of smooth semiconductor films on lattice matched insulating oxides.

As such, with the invention, a lattice-matched or near lattice-matched epitaxial oxide film is grown on a substrate (e.g., silicon or germanium). This oxide could be from the bixbyite, calcium fluorite, or pyrochlore structural classes, or it could be from the perovskite or perewskite structural classes. The important thing is that the material possesses an epitaxial relation with the underlying substrate (e.g., some of these oxides and their growth techniques are described above). The thickness of this oxide film can be from about 0.3 nm to about 2000 nm nominally, or even higher. Again, it is noted that instead of a silicon substrate, a germanium substrate can be employed.

Turning now to the method 1400, in a first optional step 1401, the oxide/substrate (e.g., silicon or germanium) is exposed to an O_2 beam.

In a step 1402, the oxide on the substrate (e.g., silicon or germanium) is cooled down to a predetermined low temperature in a vacuum system for deposition of an amorphous semiconductor. The specific temperature depends upon the semiconductor to be used.

For example, for Si it will be less than 500 C and for Ge it will be less than 300 C. A key aspect to this deposition is that the substrate temperature is low enough that the deposited silicon assumes an amorphous microstructure. Ideally, the lower the temperature the better, and preferably depositions are performed at room temperature.

In step 1403, a thin layer of semiconductor material (e.g., silicon, germanium, etc.) is then deposited upon the epitaxial oxide layer at room temperature.

Hereinbelow, using Si only for exemplary purposes and ease of description and not for limiting the invention in any way, the description of the method will proceed. However, it is noted that the inventive method has been performed using germanium.

The amorphous layer can be of any thickness. However, ideally it should be less than about 20 nm. In most applications, films of interest are only about 1-50 nm in thickness.

After amorphous semiconductor (e.g., Si, Ge, etc.) deposition, in step 1404, the amorphous silicon/oxide/substrate (e.g., Ge, Si, etc.) structure is gradually heated up to a temperature where the silicon starts crystallizing

YOR920010368US2

epitaxially. In this case, the seed for epitaxial crystallization is provided by the underlying crystalline oxide template. Above approximately 550C, the amorphous silicon layer transforms to a single crystal epitaxial layer due to solid phase epitaxial growth seeded by the oxide surface below.

In the above-described way, the resulting solid phase epitaxial growth results in a rough silicon surface. However, in order for the solid phase epitaxy to proceed with a smooth silicon surface, the annealing for solid phase epitaxy preferably is performed in the presence of a vapor or flux of a surfactant such as antimony, magnesium, As, Be, Bi, P, B, N, Ga, Al, Si, C, and In.

It is noted that using the surfactant is a well-known method as described for example, in "Surfactants in epitaxial growth", M. Copel, M. C. Reuter, E. Kaxiras, R.M. Tromp, Phys. Rev. Lett. V63, 632 (1989).

As a result, a monolayer or less of the surfactant (antimony, etc.) covers the silicon surface, passivates it and prevents it from roughening. In this fashion, high quality silicon and germanium films have been grown on LaYO layers (e.g., the subject of parent Application No. 09/898,039).

Electron microscopy and diffraction images of such layers have shown that the solid phase epitaxy of silicon commences in the 540-640 C range and that for Ge commences in the 380-480 C range.

Following solid phase epitaxy, an optional step 1405 may be performed in which the structure (e.g., oxide/substrate (e.g., silicon or germanium) is again exposed to an O_2 beam.

Further, following solid phase epitaxy (and with or without the optional step 1405), the Sb layer on the Si (or Ge) is now unwanted. It can be removed

YOR920010368US2

now by exposing the surface to an atomic hydrogen beam as shown in optional
step 1406 by exposing the surface to an atomic hydrogen beam.

Atomic hydrogen beam sources are commercially available and use the
principles of either passing molecular H_2 over a very hot filament, or passing it
through a remote radio frequency (RF) plasma source. The hydrogen reduces
Sb, and forms volatile SbH_3 that vaporizes. As noted above (e.g., in optional
step 1405), it can be useful to oxidize the Sb prior to its reduction with H_2 as
well. The inventors have produced X-ray photoelectron spectroscopy data
that shows the removal of the surface Sb as a result of the hydrogen reduction.

Solid phase epitaxy of silicon itself is not new, neither is the knowledge
of surfactant passivation of surfaces for smooth layers.

However, the novel aspects of the above method include: (i) in this case
the solid phase epitaxy of the silicon is seeded by a crystalline oxide that was
grown underneath, resulting in a silicon/epitaxial oxide/smooth epitaxial silicon
or germanium film; (ii) this solid phase epitaxy is carried out in the presence of
a vapor of a surfactant, and (iii) that an in-situ method has been discovered for
removing the surfactant by reducing it with hydrogen once its role is over.

The surfactant alters the surface energy of the silicon, such that it does not
roughen as a result of the solid phase epitaxy. Once the solid phase epitaxy has
proceeded to completion, at the substrate temperature of above about 550 C,
the surfactant vapor can be turned off.

As noted above, it may also be desired that following the oxide growth, an
optional step 1405 is performed such that the oxide/silicon (or germanium)
substrate is exposed to a molecular O_2 beam. This is performed if it is desired

YOR920010368US2

to grow a thin, amorphous silicon oxide layer at the interface between the crystalline oxide and silicon layer. It is typically carried out with the sample at a temperature of above 600 C in the deposition chamber in the presence of oxygen. The O_2 diffuses through the crystalline oxide layer and reacts with the

5 Si forming a silicon oxide layer at the interface. This operation then results in a silicon substrate/silicon oxide/lattice matched oxide/Si (or Ge) smooth epitaxial film. One reason to do this is to form a pliant amorphous layer at the interface to accommodate film stresses.

Antimony (Sb) is but one example of a surfactant that can be used. The

10 present inventors have found that other surfactants that can be used are As, Bi, P, B, N, Ga, Al, and/or In.

The present inventors have demonstrated these results using Si and Ge. The same can be done with GaAs. Only in this case, the surfactant would be one of Mg, Be, Si, C, Sb, As, and/or N.

15 Returning now to Figure 1A, the method 100 is completed, and the completed structure 200B is as shown in Figure 2B.

That is, in Figure 2B, silicon wafer 210 has the optional buffer layer 220 formed thereon. Then, the inventive compound $(La_xY_{1-x})_2O_3$ 230 is grown on the buffer layer 220 (or directly on the wafer 210), and a top silicon layer 240

20 is deposited on the inventive compound $(La_xY_{1-x})_2O_3$ 230. Such a structure would be a silicon-on-insulator structure. It is noted that the invention in its most basic form is the inventive compound 230 formed directly on the silicon wafer 210, as shown in Figure 2A.

It is noted that the invention can be advantageously used to build multilayer stacks. That is, a stack could be built having a plurality of layers.

For example, Figure 3 illustrates a structure 300 similar to that of Figure 2B but in which an additional oxide layer 330 (which can have substantially or identically the same constituents as oxide layer 230, or in which a compound different from that of 230 can be used as described below) has been grown on top of the silicon layer 240, and then an additional silicon layer (not illustrated) would be formed, and so forth. It is noted that the layers of the figures are not necessarily drawn to scale.

In the structure of Figure 3, a Silicon quantum well (240) is formed, if the thickness of well 240 is less than about 20nm. This quantum well can be the building block for resonant tunneling and light emitting devices.

Additionally, a resonant tunneling structure could be formed by forming the structure shown in Figure 3, but by further forming another silicon layer 250 over oxide layer 330. The device would be based upon electrical current tunneling from Si layer 220 to layer 250, via the oxide layers and mediated by the Si quantum well 240.

Other resonant structures may be made by depositing additional oxide and Si layers 250, 340 and 260. If layers 250 and 240 are < 20nm thick, then a dual quantum well tunneling structure is produced and so on.

Thus, the inventors have grown an oxide/silicon multilayer structure that is an epitaxial heterostructure. Such a plurality of interleaved layers/structures can be used for novel devices.

For example, the inventive compound can be used for a gate dielectric for a metal oxide semiconductor field effect transistor (MOSFET) by taking silicon and growing an insulator on it, and then growing an epitaxial silicon layer on the insulator. If this epitaxial Si layer forms the channel of a transistor, then a

5   silicon-on-insulator FET is formed.

Further, as alluded to above, the invention can be used to form a silicon on-insulator-based transistor with a gate dielectric on either side, or the inventive structures can be used for resonant tunneling devices (which are not transistors but are other devices) as briefly described above.

10   Additionally, the inventive structure could be used for an optical device in that the novel compound/silicon structure may be luminescent.

As an example of a multi-layer stack utilizing the structure of Figure 3, with the Si layer 240 being less than 20nm, a Si quantum well can be obtained, or a Si/oxide stack can be repeated, with the individual layer thickness being

15   less than 5 nm, so that a super lattice structure that acts as a luminescent material is obtained.

Further, it is noted that the present invention is not limited to a mixed rare earth oxide of $(La_xY_{1-x})_2O_3$. The present invention also is equally applicable to other rare earth materials which could be fitted into the same philosophy in

20   terms of looking at the lattice constants and matching them so that they could match silicon. Some other candidate materials and oxides which could be used are samarium (e.g., $(Sm_xY_{1-x})_2O_3$), cerium $(Ce_xY_{1-x})_2O_3$), Gadolinium $(La_xGd_{1-x})_2O_3$), Gadolinium oxide and Europium oxide (e.g., $(Gd_xEu_{1-x})_2O_3$), etc.

With the unique and unobvious aspects of the invention, new compounds have been developed in which as the yttrium oxide is growing a small amount of lanthanum (or other rare earth material as noted above) is added. The invention would find great benefit in microdevice structuring etc., due to its lattice matching with silicon.

5

While the invention has been described in terms of several preferred embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.

YOR920010368US2